REMARKS

Claims 35-67 remain pending. Independent claims 35, 45, and 57 have been amended to further clarify Applicant's invention and dependant claims 36, 38, 40, 41, 47, 49, 51, and 53 have been amended to properly reflect the amendments made to claims 35 and 45. Reconsideration of this application in light of the amendments and the following remarks and the allowance of this application are respectfully requested.

Objection to the Drawings

The Examiner has objected to the drawings as failing to show every feature of the invention specified in the claims. Particularly, the Examiner has objected to the drawings as failing to show the ball grid array wherein the ball-grid array of the first and second IC packages are conductively bonded.

Applicant respectively submits that Figures 29, 30, 35, and 36 show the ball-grid array of the first and second IC packages being conductively bonded. In Figures 29 and 30, as described in the specification in paragraph [0071],

> [r]eferring now to Fig. 29, a seventh embodiment electric module utilizes a sixth embodiment carrier 2901 designed for the mounting of multiple ball-grid array IC packages 2902. Such packages employ pads, rather than leads, to make connection from a semiconductor chip to the external world. This carries 2901 incorporates butt-l-joint leads 2903, which are solder reflowable for mounting to pads on a printed circuit board. Each of the ball-grid array IC packages 2902 has a plurality of connection elements, which in this case are pads, 2904 on each of which a metal (e.g., gold) ball 2905 has been bonded or solder reflow attached. Referring now to FIG. 30, each of the ball-grid array IC packages 2902 has been mounted on the carrier 2901 and each of the balls 2905 is physically and electrically bonded to a corresponding pad 2906 on the carrier 2901. Bonding can be via solder reflow, via vibrational energy input, or any other known technique. The mounting process has created a multiple ball-grid array package unit 3001. (emphasis added).

Additionally, in Figures 35 and 36, as described in the specification in paragraph [0073.1]

> [r]eferring now to FIG. 35, a seventh embodiment electronic module utilizes a sixth embodiment carrier 3501 designed for the mounting of multiple ball-grid array IC packages 3502 A-D. Such packages may

> employ pads, rather than leads, to make connection from a semiconductor chip to the external world. This carrier 3501 incorporates a ball-grid array 3503, which is solder reflowable for mounting to pads on a printed circuit board. Each of the ball-grid array IC packages 3502 A-D may have a plurality of connection elements, which may, for example include pads on each of which a metal (e.g., gold) ball 3505 may be bonded or solder reflow attached. Each of the ball-grid array IC packages 3502 may be mounted on the carrier 3501 and each of the balls 3505 may be physically and electrically bonded to a corresponding pad on the carrier 3501. Bonding can be via solder reflow, via vibrational energy input, or any other known technique. The mounting process creates a multiple-package ball-grid array package unit 3601, shown in FIG. 36. (emphasis added)

Based on the above showing, Applicant submits that these drawings show every feature of the claimed invention, and therefore, requests that this objection be withdrawn.

Claim Rejection under 35 USC § 103

In the Office Action, the Examiner rejected claims 35-36, 38-43, 45-47, 49-51, 54-62, and 64-67 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Vakilian (US 6,160,718, previously cited, hereinafter, Vakilian) and in view of Kim (US 6,029,025, previously cited, hereinafter, Kim).

Examiner correctly notes that Vakilian does not disclose using a ball-grid array to connect the chip to a carrier. Examiner cites to Kim to provide the support for this additional element not found in Vakilian, but Applicant respectfully disagrees, however, that there is any motivation to combine these two patents. First of all, as explained in Applicant's May 2, 2007 Response to Office Action of November 2, 2006, the substrate taught by Vakilian is purposefully missing directly under or above the package to which it is to be bonded. (See Vakilian Fig. 5, Item 12; Col. 4, line 60-62 ("the opening 14 can be formed by removing the appropriate portions of the substrate 12 by cutting, lasering, or other methods.").) This affirmative need by Vakilian to remove the substrate material from beneath the IC package effectively teaches away from any suggestion to have connecting points, such as a mounting pad array as in the claimed invention, directly beneath the IC package. (See Specification, Figs. 29 and 35.) It is well understood to

one ordinarily skilled in the art that that one purpose for an IC package having a ball-grid array is to be electrically connected to the carrier pads that are directly beneath the IC package and thereby minimizing the IC package footprint. It would not be possible to connect to this open space in Vakilian, therefore there cannot be any motivation to combine Kim with Vakilian to accomplish the claimed invention. Thus, one ordinarily skilled in the art would not find it obvious to combine Vakilian with Kim, or any other art teaching mounting pad arrays, to create the claimed invention.

Secondly, what is shown in Fig 6 of Kim is not a combination of packages, and the combination of the Vakilian with Kim would, therefore, not result in the claimed invention. Fig. 6 is described by Kim as "a sectional view illustrating another embodiment of a semiconductor device *package*." (Kim, Col. 4, lines 49-51 (emphasis added).) Within that package are chips. (See id. at Fig. 6; Col. 4, lines 52-58.) The *chips* are electrically connected through bumps. (See id. at Fig. 6; Col. 4, lines 65-67.) The examiner has not identified where Kim teaches *packages* (rather than merely chips) being conductively coupled to opposite sides of a carrier by a ball grid array. Rather, Kim only teaches leads extending out of an IC package, (see id at Fig. 6, Item 64; Col. 3, lines 32-39). Therefore, because neither Vakilian nor Kim teach integrated circuit packages conductively coupled to opposite sides of a carrier by a ball grid array, the combination of the two patents would not teach every feature of the claimed invention. As explained above, such a combination would not be possible by the teachings of Vakilian and should, therefore, not be obvious.

For the foregoing reasons, the combination of Vakilian and Kim does not teach all of the features of the claimed invention and do not possess any teaching, suggestion, or motivation to combine features of the two inventions to create the claimed invention. As such, Applicant believes that independent claims 35, 45, and 57 are in allowable form and respectfully requests Examiner to withdraw its rejection of these claims.

Further, applicant submits that independent claims 35, 45, and 57 are patentable and that dependent claims 36-44, 46-64, and 66-67 dependent from independent claims 35, 45, and 65, respectfully, or claims dependent therefrom, are patentable at least due

to their dependency from an allowable independent base claim.

Applicant respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 35, 45, and 57 in condition for allowance. Applicant submits that the proposed amendments of claims 35, 45, and 57 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicant respectfully points out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment would allow the Applicant to reply to the final rejections and place the application in condition for allowance.

Finally, Applicant submits that the entry of the amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

In view of the foregoing remarks, Applicant submits that the claimed invention, as amended, is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicant therefore requests the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this reply, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 04-0952.

Respectfully submitted,

Dewey & LeBoeuf LLP

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